REMARKS/ARGUMENTS

Claims 22-52 and 62-67 are pending in this application. Claims 27, 28, 34, 43, 45, 48, 50-52, and 67 have been withdrawn by the Examiner as being directed to a non-elected Species. By this Amendment, Applicant amends claims 22 and 40.

Applicant respectfully requests that the Examiner rejoin and allow withdrawn claims 27, 28, 34, 43, 45, 48, 50-52, and 67 when generic claims 22 and 40 are allowed.

Claims 22-26, 29-33, 35-42, 44, 46, 47, 49, 62, 63, 65, and 66 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanaka et al. (U.S. 6,251,712) in view of Makita et al. (U.S. 2005/0170573). Claim 64 was rejected under U.S.C. § 103(a) as being unpatentable over Tanaka et al. in view of Makita et al., and further in view of Zhang et al. (U.S. 5,481,121). Applicant respectfully traverses the rejections of claims 22-26, 29-33, 35-42, 44, 46, 47, 49, and 62-66.

Claim 22 has been amended to recite:

> "A method for manufacturing a semiconductor device, comprising the steps of:
>
> providing an amorphous semiconductor film including a catalyst element in at least a portion thereof, the catalyst element being capable of promoting crystallization of the amorphous semiconductor film;
>
> performing a first heat treatment on the amorphous semiconductor film so as to crystallize at least a portion of the amorphous semiconductor film, thereby obtaining a semiconductor film including a crystalline region;
>
> patterning the semiconductor film to form an island-shaped semiconductor layer including the crystalline region;
>
> forming a gate insulating film on the island-shaped semiconductor layer;
>
> **selectively thinning or selectively removing only a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed**;
>
> forming a gettering region capable of attracting the catalyst element in a region outside the region of the island-shaped semiconductor layer where the channel region, the source region, and the drain region are formed;
>
> doping the crystalline region of the island-shaped semiconductor

> layer with an impurity for forming the source region and the drain region; and
>
> performing a second heat treatment so as to move at least a portion of the catalyst element in the island-shaped semiconductor layer to the gettering region." (emphasis added)

Applicant's claim 40 recites method steps similar to the method steps recited in claim 22, including the above emphasized method step. Support for the above amendment can be found in, for example, Figs. 1D-1E, 2D-2E, 4A-4B, 6A-6B, 8A-8B, 12B-12C, and 14B-14C of the originally filed drawings.

With the improved method steps of claims 22 and 40, Applicant has been able to simplify the manufacturing process of a semiconductor device by providing a dedicated gettering region separate from the source region and the drain region in order to optimize the doping of the source region and the drain region and without adversely increasing the resistance of the source and drain regions so that they will no longer function as a source region and a drain region while significantly improving the gettering capability of the gettering region (see, for example, paragraph [0115] on pages 45 and 46 of the originally filed specification).

The Examiner alleged that Tanaka et al. teach "selectively thinning or selectively removing a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed (see fig. 4E)." Applicant respectfully submits that the Examiner has misinterpreted the step of "**selectively** thinning or **selectively** removing only a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed." One of ordinary skill in the art would understand that this step means thinning or removing the portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region **to the exclusion** of thinning or removing any other portion of the gate insulating film.

Nevertheless, claim 22, and similarly claim 40, has been amended to recite the step of "selectively thinning or selectively removing **only** a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed."

In contrast to Applicant's claims 22 and 40, Tanaka et al. teach removing a portion of the gate insulating film (407) that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed, **and also** removing a portion of the gate insulating film on the island-shaped semiconductor layer including the source region (417) and the drain region (418). See Fig. 4E of Tanaka et al. which shows the gate insulating film (407) removed from above the source and drain regions (417, 418).

Thus, Tanaka et al. fail to teach or suggest the step of "selectively thinning or selectively removing only a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed," as recited in Applicant's claim 22, and similarly in claim 40.

Makita et al. teach thinning a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed, **and also** removing a portion of the gate insulating film on the island-shaped semiconductor layer including the source and drain regions (412n, 413n). See Fig. 5F of Makita et al. which shows the gate insulating film (409) removed from above the source and drain regions (412n, 413n).

Thus, Makita et al. fail to teach or suggest the step of "selectively thinning or selectively removing only a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed," as recited in Applicant's claim 22, and similarly in claim 40.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 22 and 40 under 35 U.S.C. § 103(a) as being unpatentable over Tanaka et al. in view of Makita et al.

Zhang et al. was relied upon to allegedly cure the deficiencies of Tanaka et al. and Makita et al. However, Zhang et al. fail to teach or suggest the step of "selectively thinning or selectively removing only a portion of the gate insulating film that is located outside a region of the island-shaped semiconductor layer where a channel region, a source region and a drain region are formed," as recited in Applicant's claim 22, and similarly in claim 40.

Accordingly, Applicant respectfully submits that Tanaka et al., Makita et al., and Zhang et al., applied alone or in combination, fail to teach or suggest the method steps recited in Applicant's claims 22 and 40.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 22 and 40 are allowable. Claims 23-26, 29-33, 35-39, 41, 42, 44, 46, 47, 49, 62-66 depend upon claims 22 and 40, and are therefore allowable for at least the reasons that claims 22 and 40 are allowable.

In addition, as noted above, claims 22 and 40 are generic. Accordingly, Applicant respectfully requests that the Examiner rejoin and allow withdrawn claims 27, 28, 34, 43, 45, 48, 50-52, and 67 when generic claims 22 and 40 are allowed.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a ONE-month extension of time, extending to August 21, 2006 (August 19, 2006 falls on a Saturday), the period for response to the Office Action dated April 19, 2006.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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